**Cadence 实习生火热招募中**

**公司介绍**

Cadence是一家电子设计自动化 (EDA)与半导体知识产权(IP)的领先供应商。我们的定制/模拟工具帮助工程师设计构成芯片级系统(SoCs)芯片的晶体管、标准单元和IP模块。我们的数字工具可对千兆级、千兆赫兹及最新半导体工艺节点的SoC进行自动化设计和验证。我们的IC封装和PCB工具可实现完整的电路板和子系统的设计。

Cadence还提供用于存储器、接口协议、模拟/混合信号组件和专业处理器设计IP和验证IP不断增长的产品。在系统层面，Cadence提供一个集成的硬件/软件套件协同开发平台。总之，Cadence的创新技术在创造改变生活的重大电子产品中起着至关重要的作用。

Cadence作为全球EDA行业的领军人物，我们为优秀的你提供有竞争力的薪酬福利，前沿的技术平台，全面系统的培训课程和畅通的职业晋升通道。同时你还将参与到众多的公益活动和多彩的员工活动中。无论是你的技术能力，外语水平，还是管理技巧，人际沟通，都能得到全方位的提升，使你在未来的工作和生活中受益良多。我们关注每一个员工的职业发展，并为之努力。

如果你热爱产品验证、软件研发、IC设计工作，热衷探索EDA最前沿的技术，并且喜欢国际化的团队工作氛围，那还等什么？

快快加入Cadence大家庭！简历请直接发送至：[job\_china@cadence.com](mailto:job_china@cadence.com)，Cadence将为您提供最广阔的舞台！

欢迎关注Cadence大街网主页[http://www.dajie.com/corp/1003726/project/56726](http://www.dajie.com/corp/1003726/project/56726" \t "_blank)

更多职位信息请关注Cadence中国招聘官方微信平台，微信号：**Cadence微招聘**



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**实习时间：每周保证4天，维持6个月以上**

地点：上海浦东嘉里城(7号线，花木路站)

**欢迎2017/2018年毕业的微电子、集成电路、电子信息工程等相关专业的硕士生投递，表现优秀者有机会转正。**

**实习安排：**

通过严格的面试筛选后，能接触到EDA(电子设计自动化)行业最前沿的技术，并能得到公司资深工程师的培训和指导，从中领略跨国美资企业的工作氛围与人文环境。

**投递方式：**  
If you have interest , PLS send your update CV to [job\_china@cadence.com](mailto:job_china@cadence.com)(简历投递格式：姓名+学校+申请职位+工作地点)

**数字后端产品验证实习生（上海）**

**1. Intern-Product Validation for flowQOR**

**Position Description:**

 Do flow QOR review, debugging timing, DRC, memory and TAT issues under

help of project leader.

 Write some scripts to improve efficiency

 Do data collection and analysis

 Co-work with team members to accomplish different projects

**Position Requirements:**

 MS or excellent undergraduate

 Digital IC design knowledge is necessary, statistic timing analysis knowledge is a strong plus

 Unix System knowledge, vi/TCL/TK/CSH/Perl will be plus.

 Good communication in English and Chinese, good confidence and self-motivation.

 Commitment to work as intern for at least 6 months.

**2. Intern-Product Validation for NanoRoute**

**Position Description:**

 This intern will work in Encounter Block Implemnetation Product Validation team and focus on NanoRoute. The responsibilities include:

 Assist in Cadence EDI flow developement and validation

 Validate and maintain comprehensive NanoRoute unit and flow test cases for Encounter Digital Impelementation System.

 Develope testsuites of the new features of EDI GPS functions.

**Position Requirements:**

 MS or excellent undergraduate

 Digital IC design knowledge is necessary, statistic timing analysis knowledge is a strong plus

 Unix System knowledge, vi/TCL/TK/CSH/Perl will be plus.

 Good communication in English and Chinese, good confidence and self-motivation.

 Commitment to work as intern for at least 6 months

**3. Intern-Product Validation**

**Position Description:**

 Assist in Cadence hierarchical and DB areas developement and validation

 Validate and maintain comprehensive hierarchical/Database unit and flow test cases for Encounter Digital Impelementation System.

 Develope testsuites of the new features of hierarchical and Database functional/flow solution.

**Position Requirements:**

 MS or excellent undergraduate

 Digital IC design knowledge is necessary, statistic timing analysis knowledge is a strong plus

 Unix System knowledge, vi/TCL/TK/CSH/Perl will be plus.

 Good communication in English and Chinese, good confidence and self-motivation.

4. **Intern-Product Validation for STA**

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| Position Description: | This intern will work in Innovus "Timing Analysis" Validation team. The responsibilities include: a) Assist in Cadence STA & delayCal product and engine's development and validation; b) Develop and maintain comprehensive STA test cases for Innovus System; c) Develop and maintain system and infrastructure for high productivity and efficiency with various scripting and system development techniques. | | | |
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| Position Requirements: | * MS or excellent undergraduate, Strong perl programming experience. * IC design knowledge is necessary, statistic timing analysis knowledge is a strong plus * Unix System knowledge, vi/TCL/TK/CSH will be plus * Good communication in English and Chinese, good confidence and good self-motivation. * Commitment to work as intern at least 4 days per week for more than 6 months | | | |

5.  **Intern-Product Validation for GPS**

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| --- | --- | --- | --- | --- |
| Position Description: | This intern will work in Encounter Block Implemnetation Product Validation team and focus on GPS. The responsibilities include: a) Assist in Cadence EDI flow developement and validation b) Validate and maintain comprehensive GPS unit and flow test cases for Encounter Digital Impelementation System. c) Develope testsuites of the new features of EDI GPS functions | | | |
|  |  |  |  |  |
| Position Requirements: | a)MS or excellent undergraduate b)Digital IC design knowledge is necessary, statistic timing analysis knowledge is a strong plus c)Unix System knowledge, vi/TCL/TK/CSH/Perl will be plus. d)Good communication in English and Chinese, good confidence and self-motivation. e)Commitment to work as intern for at least 6 months | | | |